SYNOPSYS®

DesignWare IP for 5G

5G, the next-generation of mobile broadband, is driving tremendous increases in data throughput for mobile applications by introducing carrier aggregation, massive MIMO, advanced modulation, and high bandwidth channels in the mmWave spectrum. Increasing data throughput adds complexity to baseband, infrastructure, and application processor technologies. To address this complexity and meet time-to-market deadlines, SoC-level designers are integrating new, innovative IP for processing, interfaces, analog, and security. Synopsys' DesignWare® IP portfolio provides trusted solutions from high-speed analog front-ends (AFEs), proven interface IP, security IP, and efficient processing capabilities to meet the demands of the most advanced 5G chipset designs.

5G is expanding cellular mobile technologies to new applications, including the billions of low-power Internet of Things (IoT) devices, and to advanced autonomous driving technologies, as well as future concepts such as Tactile Internet. These applications require sensor, memory, and chip-to-chip interfaces, processing capabilities, and low-power wireless IP solutions that deliver low-latency capabilities with high reliability.

5G MOBILE

5G is targeting speeds that compete with existing cable home broadband solutions. 3GPP has released new specifications that focus on upgrades to new mmWave bands with higher bandwidths, additional channel aggregation, and massive antenna arrays to address the high-speed requirements. To accommodate this, high-throughput SoCs and the IP solutions used in them must consider several key design requirements.

Complex Baseband Processing

5G SoCs need processing solutions that are efficient across several different workloads required in baseband solutions. Synopsys provides optimized processors, such as the ARC EV6x and DSP-enhanced ARC HS processors, that increase work completed per cycle, reducing energy consumed by these complex solutions. For custom baseband processing designs Synopsys' ASIP Designer tool enables customers to build a processor that is optimized for their unique design requirements.

High-Speed AFE

To reach the 10Gbps capabilities required, the analog front-end IP in next-generation 5G chipsets must support GHz channel bandwidth and 256QAM. The Synopsys DesignWare Data Converter IP portfolio including the state-of-the-art AFE IP, delivers very high-speed (up to several Giga Samples Per Second (GSPS)), high-resolution RFADCs and RFDACs that support a diverse set of modulation/demodulation implementations based on direct RF, zero-IF, or heterodyne architectures. These AFEs can be configured to support different MIMO arrangements, and can efficiently process the largest of the 5G channel and carrier aggregation needs. Available in the most advanced FinFET technologies, the AFEs offer a compact and low-power solution for direct RF conversion, ready for integration into the SoC for BOM-optimized implementations. With hundreds of mobile implementations for cellular RF, including 4G/LTE and WiFi, the Synopsys AFE solutions are established and trusted.

Interface IP

With the added complexities 5G introduces, SoC developers require additional expertise and resources. Therefore, designers more than ever are relying on the DesignWare IP portfolio of interface IP, enabling critical in-house resources to focus on their product differentiation and meet the demands of 5G.

In addition to standards-based single controller and PHY interface IP, Synopsys provides configurable, pre-verified DesignWare Interface IP subsystems. These IP subsystems deliver complete, complex functions that are ready to integrate into your SoC as-is or to be customized by your team or ours. The IP subsystems include single controller and PHY integrations, a combination of multiple protocols, or complete subsystems with processors and the software stack.

Available in the most advanced FinFET technologies, Synopsys offers the latest standards in MIPI, USB, LPDDR, DDR, PCIe, high speed Multi-Protocol PHYs, and more. Specific to 5G installations, the Synopsys portfolio of Multi-Protocol PHYs deliver high-quality signal integrity and advanced power management capabilities for PCIe, CCIX, JESD204, Ethernet, CPRI, and more.

Security

Security is paramount to deter a host of threats ranging from amateur online hackers to government sponsored efforts. To deter these threats, designs need to have a secure enclave that is designed from the ground up, where software and hardware expertise have been combined. Synopsys provides a suite of security solutions to handle the high speeds needed for 5G and the Trusted Execution Environments (TEEs), including integrated SIM (iSIM) solutions, needed to protect private data. tRoot™ Hardware Security Modules for iSIM deliver secure mobile connectivity to cellular IoT while security protocol accelerators provide efficient encryption and authentication for 5G/LTE algorithms.

5G INTERNET OF THINGS

To expand mobile wireless technologies to many more devices, 3GPP has defined lower bandwidth and simplified communications protocols, such as NB-IoT and LTE-M, to address the low-power and low-cost requirements of the internet of things.

Low-Power Baseband Processing

The NB-IoT standard reduces complexity by supporting a limited data rate and feature set. Consequently, compared to legacy LTE modems, a simplified hardware/software architecture that employs a single small CPU/DSP processor for executing a complete NB-IoT software stack including the PHY layer can be used. Efficient and optimized processors such as the DSP-enhanced ARC EMxD increase the amount of work completed per cycle, reducing overall power for connectivity such as NB-IoT and LTE-M. The ARC EM9D processor offers a well-defined DSP instruction set, XY memory with advanced address generation, and extensibility with select custom instructions, enabling an efficient implementation of NB-IoT or any other communications protocol.

Highly optimized systems can be developed if what is to be processed is well understood. That is commonly the case for baseband modems. Due to the complexity of 5G, it is becoming more of the standard need. For those looking to design a customized processing element ideal for their needs, Synopsys' ASIP Designer tool enables development of programmable, task-optimized cores/accelerators with ultra-low power and size and high computation throughput.

Low-Power AFE

Synopsys provides ideal AFEs for single-chip LTE transceivers supporting low pin-count and low BOM cost for seamless integration into SoCs. Synopsys Data Converters for NB-IoT and LTE-M solutions support high-resolution modes for high-performance and ultra-low-power modes, including power scaling capabilities. These converters enable low sampling rates, and high oversampling rate capabilities to provide efficient and flexible solutions for low-power 5G connectivity.

System Cost Saving Interface IP

The latest protocols such as MIPI I3C, enable minimal pin connections and higher speeds to sensors, reducing systems costs. Synchronous Serial Interface (SSI) IP enables connectivity to the latest serial NOR Flash and other memory connectivity, removing pads from the die to establish non-volatile memory solutions for cost constrained devices.

Security

Partnerships with industry leaders such as Truphone enable all the needed technology for integrated SIM solutions on next-generation SoCs. The DesignWare tRoot Hardware Security Modules provide the secure enclaves to protect data privacy and secure the overall system.

5G AUTOMOTIVE (V2X)

5G will support extremely low-latency capabilities enabling controls to have feedback systems of <1ms.

Automotive SoCs are a key driver for low-latency requirements defined by the 3GPP. But automotive solutions require high quality, high reliability, and safety features that must be validated from the ground up, making IP the critical path for success. Synopsys provides a large portfolio of ASIL B and ASIL D Ready IP products and tools including interface IP, foundation IP, processors, and tools.

Processing for Safety-Critical Automotive

ARC Processors offer a variety of safety features including error-correcting code (ECC), watchdog timers, and lockstep interfaces. The ARC EM Safety Island Processor IP combined with extensive verification and safety documentation reduces time to market up saving over a year in development. ASIL Ready IP is essential for vehicle-to-everything applications targeted by the 5G specifications.

Automotive AFE

In addition to AFE use in 5G connectivity for V2X, analog-to-digital converters (ADCs) are used for automotive radar, LiDAR and cameras. To help address the need for automotive safety in high-reliable systems, Synopsys complements functionality enabling simplification of system self-testing, and generation of triggers to flag operational fails to help enable safety systems.

Reliability

Synopsys provides IP solutions with automotive grade mission profiles enabling the qualification of reliability standards such as AES-Q100. This includes the detailed documentation and reports necessary for automotive markets.

Quality

Quality management is essential to automotive and low-latency 5G. Synopsys IP is developed with a robust QMS (Quality Management System). This includes DFMEA reports, infrastructure for operational management and improvement and audits.

DesignWare IP for 5G Mobile	SoC Impact
Processor IP	
ARC HSxD	Combined CPU+DSP architecture and multicore control operations; efficient interfacing to hardware accelerators.
ARC EV6x	Wide SIMD/VLIW processor with ISA optimized for communications algorithms and machine learning.
ASIP Designer	Industry-leading tool to develop baseband processors. Deploys task-optimized processing solutions with hardware parallelism & custom datapaths while retaining programmability. Ideal to for custom application optimization.
ARC SoundWave Audio Subsystem	Includes audio processor, audio codecs, standard digital interfaces, and a complete, ready-to-use software environment that support the latest formats from Dolby, DTS, SRS and more.
Analog IP	
Analog Front-Ends	Can be configured to support different MIMO arrangements and can efficiently process the largest of the 5G channel and carrier aggregation needs.
Interface IP	
LPDDR	Controllers and PHYs support the latest LPDDR standards with lowest latency and high bandwidth.
MIPI CSI-2	Compliant with the latest MIPI CSI-2 specification with support for PPI interface to MIPI D-PHY, 64-bit pixel output format, and up to 8 data lanes at 2.5 Gbps per lane.
MIPI D-PHY	Enables direct CMOS image sensor connectivity; supports the latest specification; available in FinFET technologies.
MIPI I3C	Addresses the challenge of integrating the growing number of sensors found in today's most advanced phones; backward compatible with the I2C slave devices with data rates up to 33.4 Mbps, and dynamic address allocation.

USB / DisplayPort USB Type-C	High-performance, low-power, and area-efficient IP for cost-effective integration into SoCs proven in thousands of designs.
HDMI	Compliant with the latest HDMI 2.1 specification with HDCP 2.3 Content Protection.
Bluetooth Low Energy, Thread, and Zigbee	Concurrent wireless connectivity supporting the latest Bluetooth 5.1, Bluetooth Mesh, and future Bluetooth low energy Audio capabilities; operation minimizes process voltages for extended battery life; features on-chip transceiver matching network, which reduces the cost of external components and simplifies board design.
Security IP	
Security IP – HSM	Hardware Security Modules are standard components for mobile chipsets as the trend for embedded / integrated SIM capabilities are implemented.

DesignWare IP for 5G Infrastructure	SoC Impact
Processor IP	
ARC HSxD	Combined CPU+DSP architecture and multicore control operations; efficient interfacing to hardware accelerators.
ARC EV6x	Complete machine learning processing solutions ideal for 5G self-organizing networks.
ASIP Designer	Industry-leading tool to develop baseband processors. Deploys task-optimized processing solutions with hardware parallelism and custom datapaths while retaining programmability. Ideal to for custom application optimization.
Analog IP	
Analog Front-Ends	Can be configured to support different MIMO arrangements and can efficiently process the largest of the 5G channel and carrier aggregation needs.
Interface IP	
DDR	Supports the latest DDR5/4 standards with data rates up to 4800 Mbps.
Ethernet	PHY and controller support a range of Ethernet data rates up to 400G; support time-sensitive networking (TSN).
High-Speed SerDes	Multi-Protocol High-Speed SerDes PHY delivers high-quality signal integrity and advanced power management capabilities for PCIe, CCIX, JESD204, Ethernet, CPRI and more.
Security IP	
Security Protocol Accelerators	5G Encryption/Decryption Acceleration is required to handle the new high-speed bandwidths. Broad support for regional approved ciphers, hashes, and MAC algorithms enable flexible solutions for next gen SoCs.

DesignWare IP for 5G Internet of Things	SoC Impact
Processor IP	
ARC EMxD	DSP capabilities ideal for NB-IoT & LTE-M.
ARC Sensor and Control IP Subsystem	Pre-validated, tightly integrated (memories & peripherals) subsystem delivers significant power savings for 9D Sensor Fusion for context awareness.
ARC Data Fusion IP Subsystem	Tightly coupled PDM and I2S peripherals simplify integration of external audio devices. Accelerators for sensor processing enable navigation, and context awareness.
Analog IP	
Analog Front-Ends	Proven, configurable, ultra-low power data converters for NB-IoT & LTE-M.
Interface IP	
Bluetooth Low Energy, Thread, and Zigbee	Concurrent wireless connectivity supporting the latest Bluetooth 5.1, Bluetooth Mesh, and future Bluetooth low energy Audio capabilities; operation minimizes supply voltage for extended battery life; features on-chip transceiver matching network, which reduces the cost of external components and simplifies board design.
Security IP	
Security IP	Hardware Security Modules provide low data rate, low power solutions. Key software partnerships enable integrated SIM (iSIM) to reduce additional system costs.
Foundation IP	
Memory Compilers, Logic Libraries, and Embedded Test & Repair	Thick-oxide, always-on logic libraries provide the lowest leakage and low voltage down to 60% of VddNom. Low-power memory compilers are critical for mobile applications. STAR Memory System offers built-in self-test (BIST) and yield improvement.

Low Latency for Automotive	SoC Impact
ASIL Ready IP	Synopsys ARC Processor IP, Foundation IP, and Interface IP help accelerate ISO 26262 SoC-level functional safety assessments and reach target ASILs. LPDDR5/4/4X Controller and PHY: Low latency, multi-port memory controller and PHY supporting LPDDR5/4/4X SDRAM speeds up to 6400 Mbps.
AES-Q100	Reduce risk and development time for AEC-Q100 qualifications via simulation and verification testing.
QMS	Quality manuals, control of documents/records and established infrastructure enable a robust QMS system for quality control.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit synopsys.com/designware.

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