SYNOPSYS®

Synopsys Learning Journeys

An easy access guide to your learning

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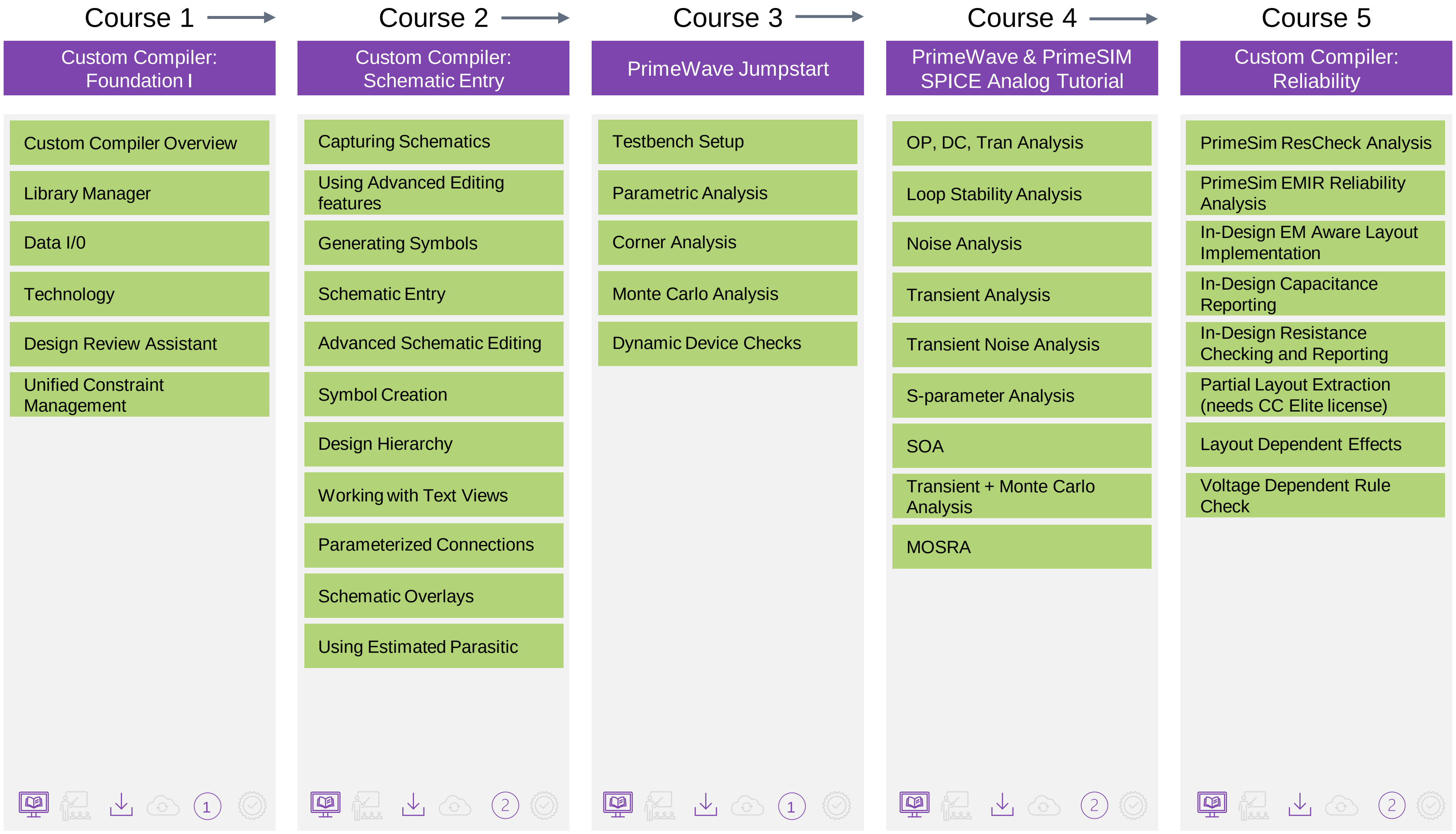
Product-based Journeys

Role-based Journeys

Custom Compiler Learning Path **Analog Designer**



Course 1 →

Custom Compiler: Foundation I

- Custom Compiler Overview
- Library Manager
- Data I/0
- Technology
- Design Review Assistant
- Unified Constraint Management

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Course 2 →

Custom Compiler: Schematic Entry

- Capturing Schematics
- Using Advanced Editing features
- Generating Symbols
- Schematic Entry
- Advanced Schematic Editing
- Symbol Creation
- Design Hierarchy
- Working with Text Views
- Parameterized Connections
- Schematic Overlays
- Using Estimated Parasitic

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Course 3 →

PrimeWave Jumpstart

- Testbench Setup
- Parametric Analysis
- Corner Analysis
- Monte Carlo Analysis
- Dynamic Device Checks

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Course 4 →

PrimeWave & PrimeSIM SPICE Analog Tutorial

- OP, DC, Tran Analysis
- Loop Stability Analysis
- Noise Analysis
- Transient Analysis
- Transient Noise Analysis
- S-parameter Analysis
- SOA
- Transient + Monte Carlo Analysis
- MOSRA

2

Course 5

Custom Compiler: Reliability

- PrimeSim ResCheck Analysis
- PrimeSim EMIR Reliability Analysis
- In-Design EM Aware Layout Implementation
- In-Design Capacitance Reporting
- In-Design Resistance Checking and Reporting
- Partial Layout Extraction (needs CC Elite license)
- Layout Dependent Effects
- Voltage Dependent Rule Check

2

Legend

- Self-paced Learning
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- Duration in Days
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Custom Compiler Learning Path **RF/Transceiver Designer**

Course 6

Custom Compiler : ICC2 CoDesign

- Data Preparation
- Analog BlackBox Preparation
- Digital Implementation
- ICC2 Editing
- Capacitance Reporting and Checking

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Legend

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Design Compiler NXT Learning Path

Course 1 → Design Compiler NXT: Jumpstart

- Introduction
- Design Setup
- Reading RTL Design
- Loading Floorplan Data
- Constraining Design
- Synthesis Techniques
- Post Synthesis Outputs

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Course 2 → Design Compiler NXT : RTL Synthesis

- Introduction to DC NXT
- Design Setup for Physical Synthesis
- Accessing Design and Library Object
- Constraints: Reg-to-Reg and I/O Timing
- Advanced Schematic Editing
- Input Transition and Output Loading
- DC NXT Ultra Synthesis Techniques
- Timing Analysis
- Constraints: Multiple Clocks and Exceptions
- SPG Flow, Congestion, Layout GUI
- Constraints: Complex Design Considerations
- Post-Synthesis Output Data
- Clk Gating/Leakage Power analysis

3

Course 3 → Design Compiler NXT : Clock Gating Low Power

- Introduction
- Power Analysis
- Power Optimization
- Clock Gating
- Advanced Clock Gating
- Self Gating
- Multibit
- ICC II Link
- Reporting

3

Course 4 → Design Compiler NXT : DFT Insertion

- Introduction
- Scan Testing and Flows
- Test Protocol
- DFT Design Rule Checks
- DFT DRC GUI Debug
- DRC Fixing
- Top-Down Scan Insertion
- Advanced Scan Insertion
- Bottom-up Scan Insertion
- Export
- On-Chip Clocking (OCC)
- DFTMAX
- Advanced Topics

2

Course 5 Design Compiler NXT: SystemVerilog for RTL Design

- Introduction
- SystemVerilog Features
- Implementing User Logic Intent
- Combinational Logic/Latches
- Meaning of full/parallel
- Registers
- State Machine
- Wildcard & Tri-state logic
- Pack/Unpack Array & Struct/Union
- Interface & Package
- Achieving High QoR-Coding

1

Legend

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Recommended Learning Journey for a **Digital Designer**

Course 1 →

Library Compiler: Foundation

- Introduction
- Functional Modeling
- Timing Modeling
- Low Power Modeling
- Modeling for Test
- Library Creation Guidelines
- CCS Modeling
- OCV Modeling
- Check Library
- Advance Node Features
- Library Analytics
- Physical Library Preparation & Creation
- Fusion Library Creation

2

Course 2 →

Design Compiler NXT: Synthesis

- Introduction to DC NXT
- Design Setup for Physical Synthesis
- Accessing Design and Library Object
- Constraints: Reg-to-Reg and I/O Timing
- Advanced Schematic Editing
- Input Transition and Output Loading
- DC NXT Ultra Synthesis Techniques
- Timing Analysis
- Constraints: Multiple Clocks and Exceptions
- SPG Flow, Congestion, Layout GUI
- Constraints: Complex Design Considerations
- Post-Synthesis Output Data
- Clock Gating/Leakage Power Analysis

3

Course 3 →

Fusion Compiler: Design Creation & Synthesis

- Introduction & GUI
- Reading RTL
- Objects, Attributes, Application Options
- Compile Flows and Setup
- NDM Cell Libraries
- Loading UPF and Floorplan
- Timing Setup & OCV
- CCD Optimization
- Power Optimization
- Additional Compile Settings and Techniques

3

Course 4 →

Fusion Compiler: Design Implementation

- Floorplanning
- Setting up CTS
- Running CTS (CCD & Classic Flow)
- Routing
- Routing DRC
- Via Ladder
- Post-route Optimization
- Signoff

2

Course 5 →

Fusion Compiler: DFT Insertion

- Introduction
- Scan Testing and Flows
- Test Protocol
- DFT Design Rule Checks
- DFT DRC GUI Debug
- DRC Fixing
- Top-Down Scan Insertion
- Advanced Scan Insertion
- Bottom-up Scan Insertion
- Export
- On-Chip Clocking (OCC)
- DFTMAX
- Advanced Topics

2

Legend

Self-paced Learning

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Recommended Learning Journey for a **Digital Designer**

Course 6 →

Fusion Compiler: SOC Design Planning

- Initial Design Planning
- IO Planning
- From Commit to Abstract Creation
- VA and Block Shaping
- Macro Placement
- PG PPNS
- Pin Placement
- Timing and Budgeting
- Integration/Assembly

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Course 7 →

Prime Time: Foundation

- Introduction to STA in PrimeTime
- STA Concepts and Flow in PrimeTime
- Methodology: Qualifying Constraints
- Methodology: Generating Reports
- Constraining Multiple Clocks
- Additional Checks and Constraints
- Correlation: POCV and AWP Analysis
- Signoff: Path Based Analysis (PBA)
- Signal Integrity: Crosstalk Delay Analysis
- Signal Integrity: Crosstalk Noise Analysis
- Timing Closure: ECO/What If Analysis
- Large Data: DMSA and Hyperscale Analysis

3

Course 8 →

StarRC: Foundation

- Extraction Fundamentals
- Gate Level Extraction
- Transistor Level Extraction
- Selective Netlist
- Field Solver
- Process Modelling
- Metal Fills

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Course 9 →

IC Validator: User (DRC & LVS)

- Setup ICV and Run DRC/LVS Testcase
- DRC Error Classification
- Execute DRC Testcase with Select Commands
- LVL
- Text Options
- Generate ICV formatted netlist
- Generate Equivalence Options
- Debug LVS Errors
- Using Short Finder

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Legend

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Recommended Learning Journey for a **Digital Designer**

Course 10 → Course 11 → Course 12

Course 10: IC Validator: Runset

- Overview
- Language Introduction
- Command API
- Writing a Simple "Flat" Rule Runset
- Running a Simple IC Validator Runset
- Advanced Programming Concepts
- IC Validator API Header Files
- Runset Coding Practices
- Layout Device Extraction
- Benefits of New Language
- Runset Structure
- Anatomy of Device Extraction Functions
- Property Calculation
- User-defined Property Functions
- Compare
- Benefits of New Language
- PXL Compare Syntax Strategy
- Anatomy of Compare Functions
- Complementary Compare Functions
- User-defined Functions
- StarRC Transistor-level Extraction Flow

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Course 11: Reference Methodology: Jumpstart

- Introduction & Overview
- Organization & Structure
- Running RM
- Demo

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Course 12: Fusion Platform Methodology: Jumpstart

- Introduction & Overview
- Organization & Structure
- Lab Example
- Installation & Setup
- FCRM for FPM Users
- FAQ – Common Topics

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Legend

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Custom Compiler Learning Path **RF/Transceiver Designer**

Course 1 →

Custom Compiler: Foundation I

- Custom Compiler Overview
- Library Manager
- Data I/0
- Technology
- Design Review Assistant
- Unified Constraint Management

1

Course 2 →

Custom Compiler: Basic Layout Design

- Layout Design Entry
- Abutment & Align Functions Advanced Editing Functions
- Hierarchical Design Creation
- Connectivity Engine
- Abstract Generation
- Design Rule Aware Editing
- Mcell Guard Ring
- Advanced Node Support
- Multi Pattern Technology
- User Defined Devices (UDD)
- Physical Verification
- Parasitic Extraction

2

Course 3 →

Custom Compiler: Accelerated Layout Design

- Schematic Driven Layout (SDL) Initialization
- SDL Placement with Connectivity Use
- SDL ECO & Cross Object Referencing
- Placement Advanced
- Symbolic Editor
- Visually Assisted Automation
- Template Manager

1

Course 4 →

Custom Compiler : Reliability

- PrimeSim ResCheck Analysis
- PrimeSim EMIR Reliability Analysis
- In-Design EM Aware Layout Implementation
- In-Design Capacitance Reporting
- In-Design Resistance Checking and Reporting
- Partial Layout Extraction (needs CC Elite license)
- Layout Dependent Effects
- Voltage Dependent Rule Check

2

Course 5 →

Custom Compiler : Automated Layout Design

- Placement Assistant
- Pin Placer
- Block Placer
- Router Introduction
- Pattern Router
- Interactive Router
- Auto Router
- Shielding
- Scripting
- Antenna Rule Support
- Technology Enablement

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DSO.ai Learning Path

Course 1

DSO: Foundation

- Introduction
- Cold Start
- Warm Start

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ESP Learning Path

Course 1

ESP: Jumpstart

- Introduction
- Symbolic Simulations
- Functional Accuracy
- PIV Introduction

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Legend

Self-paced Learning

Instructor-Led Training

Downloadable Lab

Cloud-based Lab

#

Duration in Days

Badge

Formality Learning Path

Course 1 → Course 2

Formality: Jumpstart

- Overview
- SVF Guidance
- Design Read
- Setup for Verification
- Match and Verify
- Debugging
- Formality Lab

1

Formality: Foundation

- Introduction to Equivalency checking
- Concept & Step
- Simple Logic Cones & Failing Points
- Multi-Stage Verification & SVF
- Multi-Voltage Designs & UPF
- Hard Verifications & SVP
- Efficient Debugging
- RTL & Netlist Interpretation
- Sequential Design Transforms & SVF
- Other Design Transforms & SVF
- Conclusion

2

Legend

Self-paced Learning

Instructor-Led Training

Downloadable Lab

Cloud-based Lab

Duration in Days

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Fusion Compiler Learning Path

Course 1 →

Fusion Compiler: Jumpstart

- Introduction
- Design Setup and Reading RTL Design
- NDMs/CLIBS
- Floorplan and UPF data
- Compile Flow
- Timing Setup and CCD
- Power Optimization
- Top Level Synthesis
- Design Implementation

1/2

Course 2 →

Fusion Compiler: Design Creation & Synthesis

- Introduction & GUI
- Reading RTL
- Objects, Attributes, Application Options
- Compile Flows and Setup
- NDM Cell Libraries
- Loading UPF and Floorplan
- Timing Setup & OCV
- CCD Optimization
- Power Optimization
- Additional Compile Settings and Techniques
- Hierarchical Synthesis

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Course 3 →

Fusion Compiler: Design Implementation

- Floorplanning
- Setting up CTS
- Running CTS (CCD+classic flow)
- Routing
- Routing DRC
- Via Ladder
- Post-route Optimization
- Signoff

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Course 4 →

Fusion Compiler: DFT Synthesis

- Introduction
- Scan Testing and Flows
- Test Protocol
- DFT Design Rule Checks
- DFT DRC GUI Debug
- DRC Fixing
- Top-Down Scan Insertion
- Advanced Scan Insertion
- Bottom-up Scan Insertion
- Export
- On-Chip Clocking (OCC)
- DFTMAX
- Advanced Topics

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Course 5

Fusion Compiler: UPF

- Introduction to UPF
- Power Domains
- Power Strategies
- Supply Network
- Power States
- Fusion Compiler and UPF
- Fusion Compiler Reporting

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FC/ICC II Hierarchical Design Planning Learning Path

Course 1

Fusion Compiler: SOC Design Planning

- Initial Design Planning
- IO Planning
- From Commit to Abstract Creation
- VA and Block Shaping
- Macro Placement
- PG PPNS
- Pin Placement
- Timing and Budgeting
- Integration/Assembly

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Fusion Platform Methodology Learning Path

Course 1

Fusion Platform Methodology: Jumpstart

- Introduction & Overview
- Organization & Structure
- Lab Example
- Installation & Setup
- FCRM for FPM Users
- FAQ – Common Topics

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HAPS® Hardware Learning Path

Course 1

HAPS-80: Hardware and ProtoCompiler

- Hardware Overview
- System Clocks
- HapsTrak3 Connectors
- Daughter Board and Cables
- Rack Mounting Solution
- Confpro
- HAPS ProtoCompiler Flow
- Database Concepts
- HAPS ProtoCompiler Flow Overview
- Graphical User Interface
- Introduction to Debug

1/2

Course 2

HAPS-100: Hardware and ProtoCompiler

- Hardware Overview
- System Clocks
- HapsTrak3 Connectors
- UMRBus 3.0 Overview
- Daughter Boards and Cables
- HAPS ProtoCompiler Flow
- Database Concepts
- HAPS ProtoCompiler Flow Overview
- Graphical User Interface
- Introduction to Debug

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Legend

- Self-paced Learning
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IC Compiler II Learning Path

Course 1 →

IC Compiler II: Jumpstart

- Introduction
- Design/Timing Setup
- NDMs/CLIBS
- Floorplan
- Placement & Optimization
- Clock Tree Synthesis
- Routing
- Top Level Synthesis
- Design Implementation

1/2

Course 2

IC Compiler II: Block Level Implementation

- GUI Usage (lab)
- Objects, Attributes, Application Options
- Floorplanning
- Placement
- NDM Cell Libraries
- Design Setup
- Timing Setup
- Setting up CTS
- Running CTS (CCD+classic flow)
- Routing
- Routing DRC
- Via Ladder
- Post-route Optimization
- Top Level Implementation
- Signoff

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Legend

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IC Validator Learning Path

Course 1 →

IC Validator: User (DRC & LVS)

- Setup ICV and run DRC/LVS testcase
- DRC Error Classification
- Execute DRC testcase with select commands
- LVL
- Edtext options
- Generate ICV formatted netlist
- Generate equivalence options
- Debug LVS errors
- Using Short finder
- Using VUE & ICVWB with ICV

2

Course 2 →

IC Validator: Runset

- Overview
- Language introduction
- Command API
- Writing a simple "flat" rule runset
- Running a simple IC Validator runset
- Advanced programming concepts
- IC Validator API header files
- Runset coding practices
- Layout device extraction
- Benefits of new language
- Runset structure
- Anatomy of device extraction functions
- Property calculation
- User-defined property functions
- Compare
- Benefits of new language
- PXL compare syntax strategy
- Anatomy of compare functions
- Complementary compare functions
- User-defined functions
- StarRC transistor-level extraction flow

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Course 3

IC Validatro: DRC Runset

- Writing a basic "single file" runset
- Writing debug output to OASIS/GDS Using Layer Debugger
- Understanding Error Messages & Using Diagnostic Functions
- Options Functions

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Legend

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Library Compiler Learning Path

Course 1

Library Compiler: Foundation

- Introduction
- Functional Modeling
- Methodology: Qualifying Constraints
- Timing Modeling
- Modeling for Test
- Library Creation Guidelines
- CCS Modeling
- OCV Modeling
- `check_library`
- Electromigration
- 10 nm Feature
- Library Analytics
- Physical Library Preparation
- Fusion Library Creation

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Language Learning Path

Course 1

Language: SVA Formal Verification

- Introduction to SVA
- Formal Testbench
- Coding Recommendation – Do’s and Don’ts
- Resources

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Course 2

Language: System Verilog Assertion

- Introduction
- Types of Assertions
- Action Blocks
- Disabling/Combining/Embedding Assertions
- Controlling Assertions
- Sequences and Sequence Repetition
- Sequences Operators
- Synthesis Assertion Coverage
- Assertion Libraries

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Course 3

Language: System Verilog for RTL Design

- Basic System Verilog Features
- Implementing User Logic Intent (combinatorial logic & latch)
- Implementing User Logic Intent (meaning of full and parallel)
- Implementing User Logic Intent (implementing registers)
- Implementing User Logic Intent (implementing state machines)
- Implementing User Logic Intent (wildcard and tri-state logic)
- Advanced System Verilog Features (packed or unpacked array and struct)
- Advanced System Verilog Features (System Verilog interface)
- Advanced System Verilog Features (System Verilog package)
- Achieving High QoR Through Coding

1

Course 4

Language: System Verilog Testbench

- The Device Under Test
- System Verilog Verification Environment
- System Verilog Testbench Language Basics - 1
- System Verilog Testbench Language Basics - 2
- Managing Concurrency in System Verilog
- Object-Oriented Programming: Encapsulation
- Object-Oriented Programming: Randomization
- Voltage Dependent Rule Check
- Object-Oriented Programming: Inheritance
- Inter-Thread Communications
- Functional Coverage
- System Verilog UVM preview

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Language Learning Path

Course 5

Language: System Verilog Verification using UVM

- System Verilog OOP Inheritance Review
- UVM Structural Overview
- Modeling Stimulus (UVM Transactions)
- Creating Stimulus Sequences (UVM Sequence)
- Component Configuration and Factory
- TLM Communications
- Scoreboard & Coverage
- UVM Callback
- Advance Sequence/Sequencer
- Phasing and Objections
- Register Layer Abstraction (RAL)
- Summary

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LynxNXT Learning Path

Course 1

LynxNXT: Foundation

- Introduction
- Variable Editor
- Flow Editor
- Execution Monitor
- Failure Debug
- Exploration
- Command Line Interface
- Working with FPM

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PrimeLib Learning Path

Course 1

PrimeLib: Foundation

- Tool Introduction
- Global Setting to start characterization
- Cell Level Setting to Configure Arcs
- Different Characterization flow
- Creating multiple Connect Database
- Debugging and Troubleshooting
- Complex Cell Characterization
- Timing Characterization
- Constraint Timing Characterization
- Power Characterization

1

Legend

Self-paced Learning

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# Duration in Days

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PrimePower Learning Path

Course 1

PrimePower: Jumpstart

- Power Analysis Input
- Power Components
- Leakage Power
- Internal Power
- Switching Power
- Inputs & Outputs of Power Analysis
- Simulation Activity Files
- Flow & Report

1/2

Course 2

PrimePower: Foundation

- Introduction
- Power Analysis
- Power Components
- Leakage Power
- Internal Power
- Switching Power
- Leakage & Internal Power Data
- Input & Outputs of Power Analysis
- PrimePower Analysis Modes
- Simulation Activity Files
- RTL Activity Flow
- Gate-Level Activity Flow
- PrimePower Analysis Accuracy
- PrimePower Standalone – ASCII Flow
- PrimePower – Session Based Flow
- Check & Report Power
- Report Switching Activity
- Summary

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PrimeSim Learning Path

Course 1

PrimeSim: Jumpstart

- PrimeSim Static CCK Introduction
- PrimeSim CCK Built-In Checks
- PrimeSim CCK Interactive Debugging Commands
- PrimeSim CCK False Error Pruning
- Custom Compiler – PrimeSim CCK : Setup and run

1/2

Course 2

PrimeSim: Foundation

- PrimeSim XA Introduction
- PrimeSim XA Netlist format Support
- PrimeSim XA Analyses support
- Command/Option Usage & Precedence Rules
- PrimeSim XA Post-Layout Simulation
- PrimeSim XA Command Line Usage
- PrimeSim XA Log File Details
- Accuracy and Speed Trade-off
- Back-Annotation & XBA
- Probing in PrimeSim XA
- PrimeSim XA .ALTER Usage
- PrimeSim XA .DATA Usage

2

Course 3

PrimeSim: Advance

- CCK Advanced ERC and ESD Checks
- CCK Propagation Engine – XPL and Analog Propagation
- CCK Custom Programmable Checks
- Custom Check Assertion
- GUI : Cross-Probe, Filtering, Waiver, Grouping, export

1

Course 4

PrimeSim: Advance

- Interactive Mode
- Distributed Processing
- Monte-Carlo (MC)
- MOSRA
- Aging and Self-Heating

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PrimeTime Learning Path

Course 1

PrimeTime: Jumpstart

- Overview
- PrimeTime Implementation Flow
- PrimeTime Inputs & Outputs
- Timing Analysis Flow
- Load Design & Check
- Load Library & Check
- Read Parasitic & Check
- Source Constraints & Check
- Constraints Completeness
- Coverage Analysis
- Report
- Saving & Exit

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Course 2

PrimeTime: Foundation

- Introduction to STA in PrimeTime
- STA Concepts and Flow in PrimeTime
- Methodology: Qualifying Constraints
- Methodology: Generating Reports
- Constraining Multiple Clocks
- Additional Checks and Constraints
- Correlation: POCV and AWP Analysis
- Signoff: Path Based Analysis (PBA)
- Signal Integrity: Crosstalk Delay Analysis
- Signal Integrity: Crosstalk Noise Analysis
- Timing Closure: ECO/What If Analysis
- Large Data: DMSA and Hyperscale Analysis

3

Course 3

PrimeTime: HyperScale

- Introduction HyperScale
- Flat Context Flow
- Bottom Up Flow
- Generating HyperScale Block Models
- Constraint Consistency
- Clock Mapping
- HyperScale Top-Down Flow
- HyperScale-Driven ECO
- Summary

1

Course 4

PrimeTime: Scalable STA

- Hierarchical Methodologies
- HyperScale
- HyperScale Hybrid Flow
- Distributed & Scenario Analysis
- HyperGrid
- DMSA
- DVFA/SMVA
- PBA Technologies
- Best Practices

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Legend

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- Badge

Recommend Learning Journey: **Physical Designer**

Course 1 →

Fusion Compiler: Jumpstart

- Introduction
- Design Setup and Reading RTL Design
- NDMs/CLIBS
- Floorplan and UPF data
- Compile Flow
- Timing Setup and CCD
- Power Optimization
- Top Level Synthesis
- Design Implementation

1/2

Course 2 →

Fusion Compiler: Design Creation & Synthesis

- Introduction & GUI
- Reading RTL
- Objects, Attributes, Application Options
- Compile Flows and Setup
- NDM Cell Libraries
- Loading UPF and Floorplan
- Timing Setup & OCV
- CCD Optimization
- Power Optimization
- Additional Compile Settings and Techniques
- Hierarchical Synthesis

3

Course 3 →

Fusion Compiler: Design Implementation

- Floorplanning
- Setting up CTS
- Running CTS (CCD+classic flow)
- Routing
- Routing DRC
- Via Ladder
- Post-route Optimization
- Signoff

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Course 4 →

Fusion Compiler: DFT Synthesis

- Introduction
- Scan Testing and Flows
- Test Protocol
- DFT Design Rule Checks
- DFT DRC GUI Debug
- DRC Fixing
- Top-Down Scan Insertion
- Advanced Scan Insertion
- Bottom-up Scan Insertion
- Export
- On-Chip Clocking (OCC)
- DFTMAX
- Advanced Topics

2

Course 5 →

Fusion Compiler: SOC Design Planning

- Initial Design Planning
- IO Planning
- From Commit to Abstract Creation
- VA and Block Shaping
- Macro Placement
- PG PPNS
- Pin Placement
- Timing and Budgeting
- Integration/Assembly

3

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Recommend Learning Journey: **Physical Designer**

Course 6 →

Fusion Compiler: UPF Fundamental

- Introduction UPF
- Power Domains
- Power Strategies
- Supply Network
- Power States
- Fusion Compiler and UPF

🖥 ②

Course 7

Reference Methodology: Jumpstart

- Introduction & Overview
- Organization & Structure
- Running RM
- Demo

🖥 ⤓ (1/2)

Legend

- 🖥 Self-paced Learning
- Instructor-Led Training
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- ☁ Cloud-based Lab
- (#) Duration in Days
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Reference Methodology Learning Path

Course 1

Reference Methodology: Jumpstart

- Introduction & Overview
- Organization & Structure
- Running RM
- Demo

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Legend

Self-paced Learning

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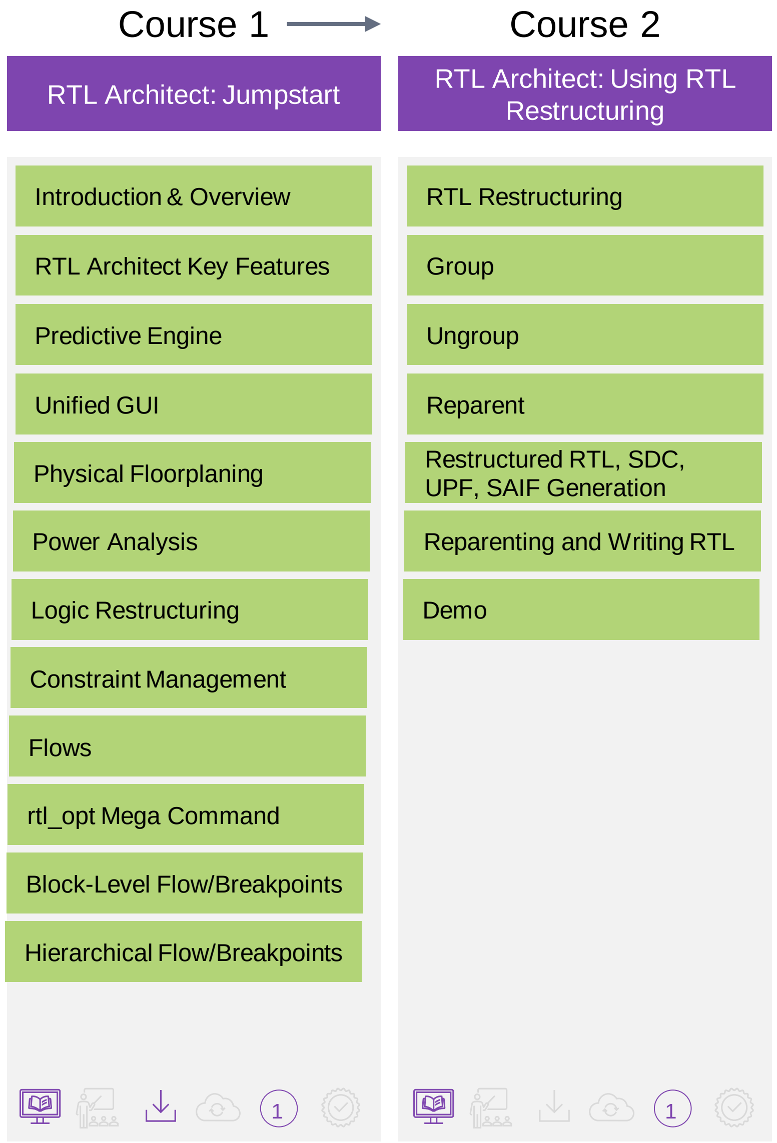
# Duration in Days

Badge

RTL Architect Learning Path



Course 1 → Course 2

RTL Architect: Jumpstart

- Introduction & Overview
- RTL Architect Key Features
- Predictive Engine
- Unified GUI
- Physical Floorplaning
- Power Analysis
- Logic Restructuring
- Constraint Management
- Flows
- rtl_opt Mega Command
- Block-Level Flow/Breakpoints
- Hierarchical Flow/Breakpoints

1

RTL Architect: Using RTL Restructuring

- RTL Restructuring
- Group
- Ungroup
- Reparent
- Restructured RTL, SDC, UPF, SAIF Generation
- Reparenting and Writing RTL
- Demo

1

Legend

Self-paced Learning

Instructor-Led Training

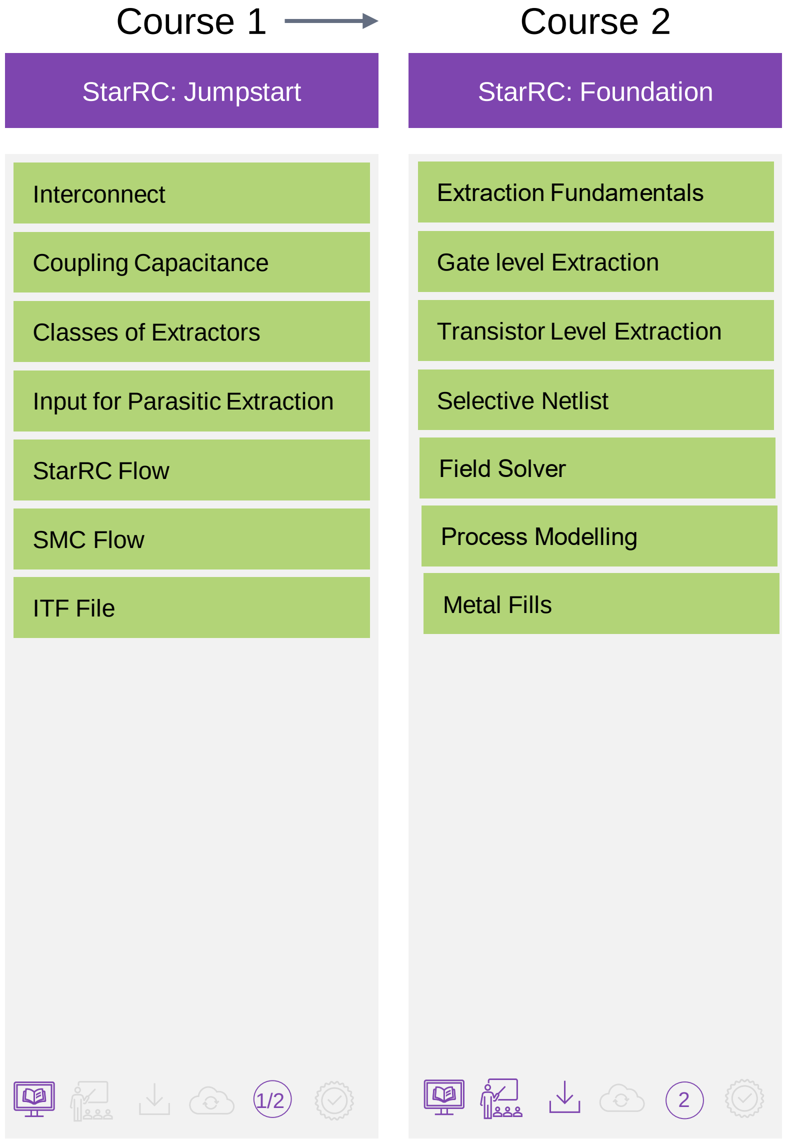
Downloadable Lab

Cloud-based Lab

Duration in Days

Badge

StarRC Learning Path



Course 1 → Course 2

StarRC: Jumpstart

- Interconnect
- Coupling Capacitance
- Classes of Extractors
- Input for Parasitic Extraction
- StarRC Flow
- SMC Flow
- ITF File

1/2

StarRC: Foundation

- Extraction Fundamentals
- Gate level Extraction
- Transistor Level Extraction
- Selective Netlist
- Field Solver
- Process Modelling
- Metal Fills

2

Legend

Self-paced Learning

Instructor-Led Training

Downloadable Lab

Cloud-based Lab

Duration in Days

Badge

SaberRD Learning Path

Course 1

SanerRD: Foundation Training Series

- Timing Domain Analysis
- Schematic Capture & Parts Library
- Operating Points & Small Signal Frequency Analysis
- Test Automation
- Design Optimization
- Introduction to Modeling
- Import SPICE Models
- Modeling with Table Look-Up
- Modeling with StateAMS
- Robust Design & Sensitivity Analysis
- Monte Carlo & Pareto
- Worst-Case Analysis
- Fault Analysis
- Stress Analysis

3

Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- Duration in Days
- Badge

Synplify: Learning Path

Course 1

Synplify: Foundation

- Introduction to Synplify Elite Flow
- Creating and Running Synplify Project
- View Log File
- HDL Analyst
- Handling High Reliability Designs
- Implementing Fault Tolerant FSMs
- ECC RAM Inferring
- Importing Quartus IP in Synplify Projects
- Debugging with SpyGlass
- Debugging with VCS
- Identify Instrumentor and Debugger

2

Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- # Duration in Days
- ✓ Badge

TestMAX Advisor Learning Path

Course 1

TestMAX: Jumpstart

- Early Testability Goals and Reports
- Debug using the GUI
- Transition Delay Checks
- Random Resistant Fault Analysis and Test Points
- Post stitch DRC Checks
- Connectivity Checks
- Flow With TestMAX Manager

1/2

Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- # Duration in Days
- Badge

TestMAX Access Learning Path

Course 1 → Course 2

TestMAX: Jumpstart

- TestMAX Access structure
- IEEE 1687 interface to drive internal instruments through TDR
- SIBs
- Define Ring configuration
- Definition of Server and Subserver
- AIT
- PDL Pattern Porting
- PDL data packetization
- Validation of AIT

1

TestMAX: ATPG

- Manufacturing Test and ATPG
- Building ATPG Models
- Running DRC
- Fault Models and Managing Faults
- Controlling ATPG
- Post ATPG Analysis
- Pattern Validation
- At-Speed Testing and Constraints
- Transition Delay Testing
- On-Chip Clocking and Compression
- Path Delay Testing
- Power Aware ATPT
- Conclusion

3

Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- # Duration in Days
- Badge

TestMAX FuSa Learning Path

Course 1

TestMAX FuSa: Jumpstart

- Functional Safety for Automotive Designs
- TestMAX FuSa: Introduction
- TestMAX FuSa: Static FuSa Analysis
- Running TestMAX FuSa: Requirement & Constraints
- Functional Safety reporting in TestMAX FuSa

1/2

Legend

Self-paced Learning

Instructor-Led Training

Downloadable Lab

Cloud-based Lab

Duration in Days

Badge

TestMAX Manager Learning Path

Course 1

TestMAX Manager: Jumpstart

- Launching and Configuring tool
- Objects, Attributes, Application Options
- NDM Cell Libraries
- Timing Setup

1/2

Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- # Duration in Days
- Badge

TestMAX SMS Learning Path

Course 1

TestMAX-SMS: Architecture

- Introduction
- SMS Wrapper
- SMS Processor
- MMB Processor
- SMS Server
- Conclusion

1

Legend

Self-paced Learning

Instructor-Led Training

Downloadable Lab

Cloud-based Lab

#

Duration in Days

Badge

TestMAX XLBIST Learning Path

Course 1

TestMAX XLBIST: Jumpstart

- LogicBIST basics
- XLBIST architecture
- XLBIST and SEQ modes of operation
- IEEE 1500 I/F and internal resources
- XLBIST patterns and interval definition
- Random Resistant Fault analysis and Test Point insertion
- X propagation analysis and fixing
- OCC and Clock Weights
- Reset Controller and Reset Weights
- Programmable SE Timing Margin
- Remap XLBIST Patterns for Debug and Diagnosis
- Validation of XLBIST patterns
- Porting of XLBIST patterns
- Simulation steps for validation
- Troubleshooting and Debug hints
- Intro to AIT

2

Legend

Self-paced Learning

Instructor-Led Training

Downloadable Lab

Cloud-based Lab

#

Duration in Days

Badge

Tweaker Learning Path

Course 1

Tweaker: ECO

- ECO Flow and Interoperability
- Basic ECO Flow
- Timing ECO
- Useful Skew Clock ECO
- Power ECO
- Area Recovery
- Reliability Recovery
- Advanced ECO Features
- Hierarchy Design Flow

3

Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- # Duration in Days
- Badge

VC Formal Learning Path

Course 1

VC Formal: Foundation

- Introduction
- Formal Verification Methodology
- SVA for Formal Verification
- VC Formal Basic
- VC Formal Navigator

1

Legend

Self-paced Learning

Instructor-Led Training

Downloadable Lab

Cloud-based Lab

Duration in Days

Badge

Zebu Learning Path

Course 1 →	Course 2
Zebu: Foundation	**Zebu: Advanced**
Introduction to Emulation	Transactors – Guide to integration + List
ZeBu overview (HW and SW)	Low Power emulation
ZeBu Ecosystem	Virtual Host and Devices
ZeBu Compile	ZeBu Debug
ZeBu Runtime	Hybrid Emulation
Tuning ZeBu for High Performance / TAT / Capacity	ZeBu Empower – SW based power analysis
Gate Level emulation	Real world interfaces with speed adaptors
1	1

Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- # Duration in Days
- Badge

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